Systems, LNCS Vol. 1055, 397–401 (1996).

[3] Godefroid P. Partial-order methods for the verification of concurrent systems. An approach for state-explosion problem, LNCS Vol. 1032, 143 p. (1996).

[4] Gerth R., Kuiper R., Peled D., Penczek W. A partial order approach to branching time logic model-checking. *Proc. 3rd Israel Symposium on Theory of Computing and Systems* (1994).

[5] Merlin P., Faber D. J. Recoverability of communication protocols. *IEEE Trans. of Communication,* COM-24(9) (1976).

[6] Roux J-L., Berthomieu B. Verification of local area network protocol with Tine, a software package for time Petri nets. *7th European Workshop on Application and Theory of Petri Nets,* 183–205 (1986).

[7] Yoneda T., Shibayaama A.,Schlingloff B.H., Clarke E.M. Efficient verification of parallel real-time systems. *Proc. 5th International Conference on Computer Aided Verification,* LNCS Vol. 697, 321–333 (1993).

Investigating Equivalence Notions for Time Petri Nets[17]

Irina B. Virbitskaite and Igor V. Tarasyuk
Institute of Informatics Systems, Siberian Division of the Russian Academy of Sciences, 6, Acad. Lavrentiev ave., 630090, Novosibirsk, Russia.
E-mail: {virb,itar}@iis.nsk.su

An important ingredient of every theory of concurrency is a notion of equivalence between systems. Typically, equivalences are used in the setting of specification and verification both to compare two distinct systems and to reduce the structure of a system. Over the past several years, a variety of equivalences — most notably, perphars, trace and bisimulation ones — have been promoted, and the relationship between them has been quite well-understood (see, for example, [Gla93]).

Those untimed equivalences abstract away from timed aspects of system behaviours. Recently, a growing interest can be observed in modelling real-time systems which imply a need of a representation of the lapse of time. Several formal methods for specifying and reasoning about real-time systems have been proposed in the last years, whereas the incorporation of real time into equivalence notions is less advanced. There are a few papers (see [ACD90,Cer93] among others) where decidability questions of timed equivalences are investigated. In these studies, real-time systems are represented by timed automata, containing fictitious time measuring elements called clocks. However, concurrency can not be modelled directly by such timed states graphs. On the other hand, time Petri nets (time nets) were considered in [MF76] to model real-time systems over dense time domain. Our main point here is to introduce timed, untimed and region equivalences in the trace (denoted by '$\equiv$') and bisimulation (denoted by '$\underline{\leftrightarrow}$') cases and establish the interrelations between these notions in the framework of time nets. Timed equivalences [Cer93] (subscribed by 't') can measure the exact real-numbered duration of every delay, whereas untimed ones [Cer93] (sub-

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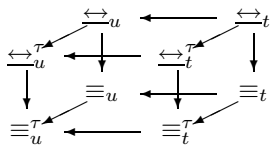

FIG. 10. The interrelations of the equivalences

scribed by 'u') do not. Region equivalences (subscribed by 'r') partition the states of a time Petri net into the so-called 'regions' [ACD90]. We also treat weak variants [Gla93] of these equivalences (superscribed by 'τ') which take into consideration 'invisible' nature of the silent action τ.

The following theorem establishes the interrelations between the timed and untimed variants of the equivalences.

Theorem 1.0.1 *Let* $\leftrightarrow, \twoheadleftarrow\!\!\twoheadrightarrow \in \{\equiv_t, \underline{\leftrightarrow}_t, \equiv_u, \underline{\leftrightarrow}_u\}$ *and* $\star, \star\star \in \{., \tau\}$ *(the symbol '.' denotes "nothing"). For time nets* N *and* N'*:* $N \leftrightarrow^\star N' \;\Rightarrow\; N \twoheadleftarrow\!\!\twoheadrightarrow^{\star\star} N'$ *iff in the graph in Figure 1 there exists a directed path from* $\leftrightarrow^\star$ *to* $\twoheadleftarrow\!\!\twoheadrightarrow^{\star\star}$*.*

We next show the coincidence of the timed equivalences with the region ones. This provides a tool to reduce the number of states of a time net implying the simplification of timed equivalences checking.

Theorem 1.0.2 *Let* $\leftrightarrow \in \{\equiv, \underline{\leftrightarrow}\}$ *and* $\star \in \{., \tau\}$ *(the symbol '.' denotes "nothing"). For time nets* N *and* N'*:* $N \leftrightarrow^\star_t N' \;\Leftrightarrow\; N \leftrightarrow^\star_r N'$*.*

For untime nets, a subclass of time nets obtained by taking delay times of the transitions equal to zero's, the coincidence of the timed and untimed variants of the equivalences is established.

Theorem 1.0.3 *Let* $\leftrightarrow \in \{\equiv, \underline{\leftrightarrow}\}$ *and* $\star \in \{., \tau\}$ *(the symbol '.' denotes "nothing"). For untime nets* N *and* N'*:* $N \leftrightarrow^\star_u N' \;\Leftrightarrow\; N \leftrightarrow^\star_t N'$*.*

We finally treat the question of preservation of the considered equivalences under a special case of transition refinement (a modification of SM-refinement [BDKP91] for time nets, where transitions are replaced by time state-machine nets). The following theorem demonstrates which of the equivalences are preserved under time SM-refinement.

Theorem 1.0.4 *Let* $\leftrightarrow \in \{\underline{\leftrightarrow}_t, \underline{\leftrightarrow}_u\}$*. For time nets* N *and* N' *s.t. some their transitions are labelled by the visible action* a *and time SM-net* D*:* $N \leftrightarrow N' \;\Rightarrow\; ref(N, a, D) \leftrightarrow ref(N', a, D)$*.*

References

[ACD90] Alur R., Courcoubetis C., Henzinger T.A. *The observational power of clocks.* LNCS **836**, pp. 162–177, 1994.

[BDKP91] Best E., Devillers R., Kiehn A., Pomello L. Concurrent bisimulations in Petri nets. *Acta Informatica* **28**:231–264, 1991.

[Cer93] Čerāns K. Decidability of bisimulation equivalences for parallel timer processes. LNCS **663**, pp. 302–315, 1993.

[Gla93] van Glabbeek R.J. The linear time – branching time spectrum II: the semantics of sequential systems with silent moves. Extended abstract. LNCS **715**, pp. 66–81, 1993.

[MF76] Merlin P., Farber D.J. Recoverability of communication protocols. *IEEE Transactions on Communication Protocols* **COM-24(9)**, 1976.

Temporal Logics for Concurrent Nondeterministic Processes

Irina B. Virbitskaite and A. Votintseva
Institute of Informatics Systems, Siberian Division of the Russian Academy of Sciences, 630090, Novosibirsk, Russia.
E-mail: virb@isi.itfs.nsk.su

Temporal logics have been recognized as a very convenient formalism to reason about concurrent and distributed systems. While several linear time and branching time temporal logics of different complexity and expressive power have been developed, most of them are subsumed by the logic CTL^*. In the standard definition of CTL^*, only future temporal operators are considered. In order to enhance the logic expressivity a different set of additional temporal modalities have been incorporated into CTL^* (see [3] among others). Our first aim here is to extend the CTL^* family of logics by introducing a number of new logics: CTL^*_b with backward combinators, CTL^*_c with a concurrency modality, CTL^*_a with a conflict (alternative choice) modality and CTL^*_{abc}, the combination of the above logics. Note that the logic CTL^*_b allows the specification of several interleaving pasts of any time instant, whereas the logics with backward combinators considered in the literature (see, for example, [3]) restrict themselves to dealing with a single past of a time instant. The logics proposed here can indeed express all the relations — causality, concurrency, conflict — between events of concurrent and distributed systems.

Event structures [4] provide a very detailed model for system behaviours. All features considered by the logics are represented therein. Therefore we choose these as a natural candidate for a common framework of interpretation of the logics proposed.

Since logics naturally give rise to equivalence classes consisting of all those systems which satisfy the same formulas, often the logics known from the literature have been compared with behavioural equivalences for a better understanding and evaluation. Our second aim here is to establish behavioural matches for the equivalences, induced by the above extensions CTL^*_β and denoted by '$\sim_{CTL^*_\beta}$' with $\beta \in \{a, b, c, abc\}$.

Various equivalence notions have been defined on the domain of event structures to obtain more abstract system representations. However the proposed in the literature bisimulations [2] (denoted by '$\approx$'), namely interleaving (subscripted by 'i'), step (subscripted by 's'), pomset (subscripted by 'p') and history-preserving (subscripted by 'h') variants, and backward variants of bisimulation [1] (subscripted by 'b') have turned out not to be adequate for our purpose. In order to overcome this lack, we introduce a number of bisimulations which explicitly reflect concurrency (subscribed by 'c') as well as conflict (subscribed by 'a') between events in the structures. Our third